a punch-trough stopper area that surrounds a source area and a drain area of said first MOS transistor and provides a punch-through voltage resistance between said source area and said drain area.--

--8. (Amended) The semiconductor integrated circuit device according to Claim 1, wherein said source area includes a source LDD area and said drain area includes a drain side LDD area, and wherein the punch-through stopper area has a pocket structure that encloses the source side LDD area and the drain side LDD area.--

Kindly add new claim 11 as follows:

--11. (New) The semiconductor integrated circuit device according to Claim 1, further including a well having a lower impurity concentration than that of the punch-through stopper region formed in the substrate, wherein the punch-through stopper area is formed in the well.--

REMARKS

Claims 1-8 and 11 are now pending in this application for which applicant seeks reconsideration.

Amendment

Claim 1 has been amended to clarify that the first and second MOS transistors are lateral type. Claim 8 has been amended to improve its language. New claim 11 has been added to further define the invention. No new matter has been introduced.

Art Rejection

Claims 1-8 were rejected under 35 U.S.C. § 102(b) as anticipated by Williams (USP 5,541,125). Applicant traverses this rejection because Williams does not disclose or teach a second MOS transistor having a larger channel length than a first channel.